## REMARKS

Claims 15-22, as amended, remain herein.

Applicants appreciate the statement in the Office Action that the election of species requirement has been withdrawn and all of the species examined.

Applicants appreciate the statements in the Office Action that claims 3, 5-7 and 10-14 would be allowable if rewritten in independent form to include all of the limitations of the independent claim(s) from which they depend.

Claims 1-14 have been canceled and rewritten as new claims 15-22, wherein claim 15 corresponds to claim 1; claim 16 corresponds to claims 2 and 3; claims 17 and 18 correspond to claims 3 and 4; claim 19 corresponds to claim 8; claim 20 corresponds to claim 9; claim 21 corresponds to claims 10-12; and claim 22 corresponds to claim 13.

Claim 15, in addition to the subject matter of claim 1, recites an analog signal processing means including a playback signal detection means, a serial reception means for receiving a signal transferred from the serial transfer means on the basis

of a conversion command from the A/D conversion command means of the digital signal processing means, and a signal switching means for successively selecting plural data signals obtained by the playback signal detection means, according to a signal received by the serial reception means, and for time-division-multiplexing the selected signals. See applicants' specification, page 27, lines 7-12, which state:

> A DSP (arithmetic means) 140 receives the respective signal outputted as the digital signal, and selects the respective signals in the same order as the order in which the switching circuit 10 successively selected the signals, and performs signal processing on the selected signals successively.

And, applicants' specification, page 28, lines 14-16, state:

> The A/D conversion command generation circuit 13 predetermines the order in which the switching circuit 10 selects the respective control signals.

1. Applicants respectfully request the Examiner to provide an initialed copy of PTO Form 1449 indicating receipt and consideration of references accompanying an Information Disclosure Statement filed January 30, 2002.

2. Objections were stated to claims 1, 4, 5 and 11. Each informality has been amended, thereby mooting those objections.

3. Claims 1, 2, 8 and 9 were rejected under 35 U.S.C. §103(a) over Shio JP 06-236556 and Imamura et al. U.S. Patent 4,287,802. Claims 1, 2, 8 and 9 have been canceled and rewritten as stated herein.

The presently claimed optical disk control device includes an analog signal processing means and a digital signal processing means as recited in claim 15, wherein the digital signal processing means is for successively performing a programmed order of operations. For example, it obtains a value of a register (such as an error signal in focus control while reading from an optical disk), and stores a result of a prescribed arithmetic process performed on the digital value (for example, performing phase compensation filtering arithmetic to perform closed loop disk control), and data stored in a register is simply converted to an analog signal for driving an actuator by a D/A converter.

The presently claimed controller also includes an A/D conversion means for performing A/D conversion of plural analog signals in a series of operations by transferring a conversion command of analog data to a signal switcher according to the order of digital signals to be subjected to arithmetic processing, i.e., the controller includes an A/D conversion means for analog-to-digital converting a data signal transferred from the analog signal processing means, and an arithmetic processing means for performing arithmetic processing on the basis of a digital signal outputted from the A/D conversion means, which is for generating and A/D conversion command under an instruction from the arithmetic processing means, wherein the serial transfer means is for serially transferring a command signal from the A/D conversion command means, as recited in applicants' claim 15. This arrangement is nowhere disclosed or suggested in the cited references.

Shio JP '556, columns 4-6, discloses that multiplexer 9 selects and outputs one of signals FS, FE, TE and LE, which are information signals outputted from an optical disk according to a 2-bit control signal CNT1 outputted from controller 10, and

the signal outputted from multiplexer 9 is digitized by the A/D converter, and is successively stored in registers 12-15 at intervals of cycle T, which are determined by trigger signal CNT2 outputted from controller 10. Further, Shio JP '556 discloses that the respective signals stored in the registers are transferred to the DSP, and the respective arithmetic processings are successively performed by the DSP at timings of timing signal CNT3 outputted from the controller.

That is, in Shio JP '556, the multiplexer is controlled by a 2-bit control signal CNT1 outputted from the controller, and an information signal outputted from the multiplexer is successively A/D converted. Then, the respective information signals that were A/D converted are stored successively in registers 12-15 at intervals of cycle T, which are determined by trigger signal CNT2 outputted from controller 10, and arithmetic processing is performed on the respective information signals stored in the registers in a predetermined order with a cycle of timing signal CNT3. Also, a timing signal CNT3 is counted, and the DSP is operated to change the order of the arithmetic processing according to the count value.

Signals stored in the Shio JP '556 registers are signals randomly selected by a 2-bit control signal CNT1, which are to be stored in the registers in the order of the signals selected by CNT1. Thus, when applying a system wherein multiplexer 9 does not select a signal according to 2-bit control signal CNT1 outputted from controller 10, but changes the order of selection according to a signal outputted from a serial reception means as in the presently claimed invention, it becomes impossible to find out what kind of signals are stored in the registers. This is because there is no means of communicating from the controller to the DSP the relationship between a signal to be stored and a register to store the signal.

Further, Shio JP '556 describes a disk control device that is operated with a 2-bit control signal CNT1 outputted by an instruction of controller 10, a trigger signal CNT2, and timing signal CNT3, which determines the cycle of the arithmetic processing by the DSP. Controller 10 in Shio JP '556 is merely for providing the DSP with a timing for starting an arithmetic process, and is completely different from the presently claimed structure, which performs a series of operations on the basis of

a conversion command generated from an A/D conversion command means under an instruction of the DSP, as recited in applicants' claim 15.

The Office Action cites Imamura et al. '802 as allegedly teaching serial-transferring information from one chip to another and a serial reception means for receiving the signal from the serial transfer means. But, Imamura et al. '802 does not disclose anything that would cure the deficiencies of Shio JP '556 as explained herein.

In contrast, the presently claimed optical disk control device performs switching a plurality of information signals (e.g., control signals) obtained from a play signal detection means, and performs A/D conversion and arithmetic processing on transferred information signals in a series of operations on the basis of a conversion command generated from an A/D conversion command means under an instruction of the DSP, and the information signals designated by the conversion command are operated on by an arithmetic means immediately after being stored in a designated register.

The presently claimed disk controller includes controlling a serial transfer means on the basis of a conversion command from and A/D conversion command means under an instruction of the DSP, and operating a signal switching means on the basis of a conversion command obtained from a serial reception means, which is located at the side of an analog signal processing means. That is, the controller includes a serial reception means for receiving a signal transferred from the serial transfer means of the DSP on the basis of a conversion command transferred from the A/D conversion command means of the DSP, and a signal switching means for successively selecting plural data signals obtained by the playback signal detection means, according to a signal received by the serial reception means, and for time-division-multiplexing the selected signal, as recited in applicants' claim 15. In contrast, the controller of Shio JP '556 when modified by the teachings of Imamura et al. '802, even if its structure were changed to one wherein a 2-bit control signal CNT1 outputted from the controller is replaced by a signal outputted from a serial reception means for controlling

the multiplexer, such a structure still would be different from the controller recited in applicants' claim 15.

No combination of Shio JP '556 with Imamura et al. '802 would teach or suggest applicants' digital signal processing means for successively performing arithmetic processing on a digital signal according to programmed command, i.e., an A/D conversion means for performing A/D conversion of plural analog signals in a series of operations by transferring a conversion command of analog data to a signal switcher according to the order of digital signals to be subjected to the arithmetic processing, i.e., an A/D conversion command means for generating an A/D conversion command under an instruction from an arithmetic processing means, which is for performing arithmetic processing on the basis of a digital signal outputted from an A/D conversion means of the DSP means, and a serial transfer means of the DSP means for serially transferring a command signal from the A/D conversion command means.

Claim 16 further recites a disk controller wherein the A/D conversion means is for successively selecting output signals from the signal switching means of the plural analog signal

processing means on the basis of a command from the A/D conversion command means of the DSP means, and for successively converting the selected output signals into digital signals. That is, the presently claimed controller includes an analog signal processing means that switches and multiplexes a plurality of information signals on the basis of the conversion command, which is serially transferred from a digital signal processing means according to the order of the digital signals that are arithmetically processed by the arithmetic means. The controller of Shio JP '556, even if sought to be modified by some disclosure of Imamura et al. '802 still would not have applicants' structure and could not perform applicants' processing.

For the foregoing reasons, neither Shio JP '556 nor Imamura et al. '802 contains any teaching, suggestion, reason, motivation or incentive that would have led one of ordinary skill in the art to applicants' claimed invention. Nor is there any disclosure or teaching in either of these references that would have suggested the desirability of combining any portions thereof effectively to anticipate or suggest applicants'

presently claimed invention. Claims 26-22, which depend from claim 15, are allowable for the same reasons explained herein for claim 15. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

4. Claims 1, 2 and 4 are rejected under 35 U.S.C. §103(a) over Nakamura et al. U.S. Patent 4,795,958 and Imamura et al. '802. Claims 1, 2 and 4 have been canceled and rewritten as described herein.

The Office Action cites Nakamura et al. '958 as allegedly disclosing applicants' optical disk control device. However, Nakamura et al. '958 does not disclose a serial reception means for receiving a signal transferred from the serial transfer means of the DSP on the basis of a conversion command transferred from the A/D conversion command means of the DSP, and a signal switching means for successively selecting plural data signals obtained by the playback signal detection means, according to a signal received by the serial reception means, and for time-division-multiplexing the selected signal, as recited in applicants' claim 15.

The Office Action admits that Nakamura et al. '958 does not disclose a serial transfer means for serial-transferring the command signal generated by the A/D conversion command means or a serial reception means for receiving the signal from the serial transfer means and controlling the signal selection operation of the signal switching means on the basis of the received signal, and cites Imamura et al. '802 as allegedly teaching same. And, Imamura et al. '802 does not disclose anything which would cure the deficiencies of Nakamura et al. '958 explained herein.

The presently claimed disk controller is as described herein, wherein the analog signal processing means further includes a sample hold means for sampling and holding an output signal from the signal switching means, on the basis of a signal transferred from the serial transfer means, and wherein the A/D conversion means is for converting an analog signal which is sampled and held by the sample hold means, into a digital signal, in place of an output signal from the signal switching means. This arrangement is nowhere disclosed or suggested in the cited references.

With such an arrangement, a pair of control signals can be obtained at the same time by sampling and holding a pair of information signals (control signals) obtained from the playback signal detection means at the same time, thereby realizing an effect of significantly lowering the difference error between the two signals.

To the contrary, Nakamura et al. '958 teaches, synchronized with a horizontal synchronous signal from the timing controller, generating respective timing pulses such as 1H cycle (b), 1/2H cycle(c) and 1H cycle(d) with phase differences of 1/4 H to one another. In response to timing pulses (b)-(d), the switching circuit switches the respective analog error signals, the respective time divided error signals are sampled and held synchronized with the respective timing pulses (b)-(d) in one sample hold circuit, and A/D conversion is performed.

Nakamura et al. '958 discloses a controller that outputs a timing pulse according to the horizontal synchronous signal, and samples and holds the respective error signals that are switched by the timing pulse using the signal synchronized with the timing pulse, and this sampling and holding is inserted in order

to obtain enough time for A/D conversion for the A/D conversion in the next stage.

In contrast, the presently claimed controller controls a serial transfer means on the basis of a conversion command from the A/D conversion command means in the digital signal processing means, operates the signal switching means on the basis of a conversion command obtained from the serial reception means, which is located at the analog signal processing means, and transfers a sample hold pulse to the sample hold circuit on the basis of a conversion command from the A/D conversion command means, obtained by the apparatus of claims 17 and 18. The object is optionally to change the information signals (control signals) obtained from the playback signal detection means at the same time, while providing a sample hold circuit, and therefore realizing a unique effect of significantly lowering the difference error between the two signals by obtaining a pair of information/control signals at the same time.

All claims 15-22 are now proper in form and patentably distinguished over all grounds of rejection stated in the Office Action. Accordingly, allowance of all claims 15-22 is respectfully requested.

Should the Examiner deem that any further action by the applicants would be desirable to place this application in even better condition for issue, the Examiner is requested to telephone applicants' undersigned representatives.

Respectfully submitted,

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